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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,371	03/30/2004	Katsunori Yanashima	09794353-0032	4684

26263 7590 02/28/2006

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EXAMINER	
SUCH, MATTHEW W	

ART UNIT	PAPER NUMBER
2891	

DATE MAILED: 02/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/813,371	YANASHIMA ET AL.	
	Examiner	Art Unit	
	Matthew W. Such	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-53* is/are pending in the application.

4a) Of the above claim(s) *2-15 and 29* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,16-28 and 30-53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *26 August 2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Invention I in the reply filed on 6 February 2006 is acknowledged.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 16-29 and 31-53 are rejected under 35 U.S.C. 102(e) as being anticipated by Ito et al. (`787).

4. Regarding Claims 1, 43-46, 50 and 52-53, Ito teaches a method for growing a nitride type III-V group compound semiconductor layer forming a laser light emitting diode device (Paragraphs 0056, 0109-0121 and 0167) on a nitride type III-V group compound semiconductor substrate. The substrate has a plurality of second regions in the crystal with a second dislocation density (Figs. 1A-1D, Element 25 and Figs. 2-5, Element 11) regularly arranged in a first region made of a crystal with a first dislocation density (Figs. 1A-1D, Element 25). The dislocation density of the second regions is greater than the dislocation density of the first regions (refer to

entire publication). The nitride type III-V group compound semiconductor layer is separated from the second regions in the substrate by a mask (Figs. 3-5, Element 13).

Furthermore, second regions can be stripes having first regions in the middle in a parallel direction (Paragraph 0019).

5. Regarding Claims 16 and 20-25, Ito teaches that second regions should be periodically arranged and a minimum interval of 100 microns (Paragraph 0069).

6. Regarding Claims 30 and 31, Ito teaches that the second regions can be formed as stripes or dots 10-40 microns wide (Paragraphs 0069, 0071, 0074-0075, 0085).

7. Regarding Claims 35-37, Ito teaches that the dislocation density of first regions are 10^4 to 10^5 cm^{-2} (Paragraph 0075), and that the dislocation density of second regions can be so high that it consists of a polycrystalline structure (dislocation density of second regions five times greater than the density of first regions) (Paragraph 0076).

8. Regarding Claims 27 and 32-34, Ito teaches second regions with a high dislocation density (Figs. 1A-1D, Element 25 and Figs. 2-5, Element 11) distributed among first regions (Figs. 1A-1D, Element 25) with a low dislocation density. The space between the second regions and first regions defines a third region.

The second regions have a high dislocation density (Paragraph 0076) corresponding to a concentrated density and the first regions have a low dislocation density (10^4 to 10^5 cm^{-2} as

described above) corresponding to a minimum density. Ito describes that the dislocation crystalline defect can build up in the high density regions (Paragraph 0063), leaving the third region to have a dislocation density greater than the minimum of the first region and less than the concentration of the second region.

Ito teaches that the interval between second regions can be 100-600 microns (Paragraph 0069), the diameter of the second regions can be 10-40 microns (Paragraph 0075), and the diameter of first regions, located in the middle of second regions, can be 0-30 microns (Paragraphs 0019 and 0078). By setting the diameter of first regions to 30 microns and the diameter of second regions to be 40 microns, the diameter of third regions can be 100 microns greater than the diameter of second regions if the interval between second regions is 130 microns.

9. Regarding Claim 38, Ito teaches the method of claim 27 wherein the dislocation density of first regions is in the range 10^4 to 10^5 cm^{-2} and the dislocation of second regions can approach infinity. Since the dislocations build up in second regions to high concentrations and migrate away from first regions to leave low concentrations, a concentration gradient exists through third regions, which are disposed between first and second regions. Therefore, the dislocation density of third regions falls between the dislocation density of first regions and dislocation density of second regions. Furthermore, Ito describes that the dislocation density of a GaN crystal growth by standard ELOG methods results in a defect density of approximately 5×10^7 cm^{-2} for regions not affected by a concentration fields (Paragraph 0008).

10. Regarding Claims 39-42, a substrate material having a plurality of high dislocation concentration regions can be GaN. By the claimed formula, $Al_xB_yGa_{1-x-y-z}In_zAs_uN_{1-u-v}P_v$, the subscripts x, y, z, u and v are all zero. Ito also teaches that the substrate can contain Al, Ga, In, As, N and P (Paragraphs 0051-0055).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 17-19 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ito in view of Kozaki (`618).

Ito teaches the method of claim 1, wherein a plurality of second regions can be formed periodically in a striped shape, or aligned in rows in an individually dotted formation (Paragraph 0064, 0069 and 0071). The striped masked taught by Ito are an example of irregular polygon prism shapes. Each strip extends in parallel across the entire length of a circular wafer, so each stripe has distinctive lengths and endpoint geometries depending on the relative location of the stripe. However, Ito is silent regarding precise lattice arrangement geometries for regular arrays.

Kozaki teaches a method for growing nitride type III-V compound semiconductor layers wherein a substrate can be a nitride type III-V layer having dislocation defect concentration regions arranged periodically in a stripe, grid, or island configuration (see entire publication). Masks can be arranged to form high dislocation density regions in as either islands or grids in a

hexagonal lattice pattern (Fig. 2C), rectangular or square formation, where each opening width of a rectangular pattern is the same size (Fig. 2B).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the plurality of second regions in aligned rows as described by Ito in the specific geometric lattice patterns of a hexagon, rectangle, or square as taught by Kozaki. One would have been motivated to use these configurations to simplify manufacturing processes. For example, a hexagonal lattice shape allows for III-V crystal growth in the [0001] direction with the mask aligned with the {11-22} facets or a rectangular or striped mask aligned along the [1-100] direction (Ito Paragraphs 0056-0071) causing the dislocations to spread in the growing direction and concentrate into a predetermined position (Ito Paragraph 0063).

13. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ito in view of Kozaki ('618).

Ito teaches the method of claim 27, wherein third region is disposed between first and second region. Ito teaches a mask covering the second region (Figs. 3-5, Element 13). Furthermore, Ito teaches a specific example where the second region is 40 microns wide and the mask is 50 microns wide, which covers only a portion of a third region leaving a remaining portion of a third region in direct contact with the nitride type III-V group compound semiconductor layer grown above (Paragraph 0086). However, Ito also teaches that the mask has a width wide enough to cover a dislocation concentration region and that the mask can be wider than 50 microns (Paragraph 0086). Ito does not explicitly teach a mask wide enough to cover the entire third region.

Kozaki teaches masks that cover every portion of the substrate except for periodically shaped windows through which epitaxial crystal growth occurs. The width of the window can be as 10-30 microns (Paragraph 0051).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use widths of mask windows up to 30 microns provided by Kozaki coinciding with the diameter of first regions taught by Ito, which is up to 30 microns (Paragraphs 0019 and 0078), covering both second and third regions in the substrate. This leaves only the low dislocation concentration first region open to epitaxial growth, reducing the concentration of dislocations propagating up from the substrate into the nitride type III-V compound semiconductor layer, yielding a high quality crystal.

14. Claim 47 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ito in view of Ng (Complete Guide to Semiconductor Physics).

Ito teaches the method of claim 45 and suggests that compound semiconductors are useful for a variety of optical applications including lasers, RGB projectors, optical disc drive units, optical pickup units, printers, etc. (Paragraphs 0197-0205). Ito is silent on specifically teaching using the device formed from the disclosed method to produce a photo detector.

Ng teaches that heterojunctions made from compound semiconductor materials are useful for forming self-electrooptic-effect devices (SEED), which have photo detector capability (Page 503).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the methods disclosed by Ito to produce low defect compound semiconductor

substrates and layers for the multiple quantum wells required for a photo detector application such as a SEED, disclosed by Ng (Page 503). Furthermore, the barcode reader and optical disc drive applications suggested by Ito requires both a light emission and photo detection capabilities which, if manufactured in a single chips having both light emission and photo detection capabilities would reduce manufacturing cost and complexity through increase integration.

15. Claim 48 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ito in view of Ng (Complete Guide to Semiconductor Physics).

Ito teaches the method of claim 45 and suggests that compound semiconductors are useful for power devices (Paragraph 0002), but is silent on specific examples of power devices or electron traveling devices that can be produced by the disclosed methods.

Ng teaches that heterojunction bipolar transistors have higher energy and higher velocity, reducing base transit times and resulting in a faster device (Page 280). Ng further teaches an example of a power device, such as a Darlington amplifier, which uses bipolar transistors (Page 280). The applicant discloses that a GaN type heterojunction bipolar transistor is an example of an electron traveling device (Applicant specification Page 102, Lines 25-27 and Page 103, Lines 1-2).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the methods disclosed by Ito to produce an electron traveling device such as a heterojunction bipolar transistor (useful for power applications) as described by Ng. The motivation to do so is given by Ng that the minimal lattice mismatch between various compound semiconductors make heterojunctions available (Page 280).

16. Claims 49 and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ito in view of Kozaki ('618).

Ito teaches the method of claim 1, wherein a plurality of second regions can be formed periodically in a striped shape, or aligned in rows in an individually dotted formation, which are all regularly formed but are not limited to being at identical intervals (Paragraph 0064, 0069 and 0071). However, Ito is silent regarding row direction and relative distances.

Kozaki teaches a method for growing nitride type III-V compound semiconductor layers wherein a substrate can be a nitride type III-V layer having dislocation defect concentration regions arranged periodically in a stripe, grid, or island configuration (see entire publication). Masks can be arranged to form high dislocation density regions in a rectangular formation (Fig 2B) showing a first interval in a first direction and a second interval in a second direction perpendicular to the first direction with the second interval being smaller than the first interval.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a rectangular pattern as shown by Kozaki in Fig. 2B with the second regions of Ito in order to maximize the regular distance between high dislocation density regions, leaving a regular pattern of low dislocation density regions between. The low dislocation density regions yield highly luminescent devices and the regular pattern allows for a high packing density of devices on a single wafer, as shown by Ito in Figs. 11-13.

Conclusion

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Biwa (`571),

Koike (`305),

Morita (`648),

Takeya (` 534 and `579) and

Tanaka (`712)

Each teaches various methods for concentrating dislocation density into noncritical areas to improve crystal quality of device formation areas.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew W. Such whose telephone number is 571-272-8895. The examiner can normally be reached on Monday - Friday 8AM-5PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bradley W. Baumeister can be reached on 571-272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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MWS
2/16/06

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